PENDING CLAIMS

Claim 1 (original): A semiconductor storage device having a security function for imposing limitation on data rewriting, the semiconductor storage device comprising:

at least one non-volatile memory cell array block which is capable of receiving concurrent electrical erasure;

at least one memory region, each one of said at least one memory region being provided in the at least one memory cell array block, for storing a security release key;

at least one non-volatile storage means for storing a security registration lock corresponding to each of the at least one memory cell array block;

a determination circuit for comparing a value which is generated based on the security release key against a value which is generated based on the security registration lock to determine whether or not to grant release of the security function; and

a memory cell array data output switching circuit for, when an output signal from the determination circuit indicates a matching result of comparison between the value which is generated based on the security release key and the value which is generated based on the security registration lock, permitting data which is read from a corresponding one of the at least one memory cell array block to be externally output.

Claim 2 (original): A semiconductor storage device according to claim 1, wherein:

the semiconductor storage device further comprises at least one register for retaining an output signal output from the determination circuit; and

when an output signal output from the at least one register indicates that release of the security function is to be granted, the memory cell array data output switching circuit permits data

which is read from a corresponding one of the at least one memory cell array block to be externally output.

Claim 3 (original): A semiconductor storage device according to claim 1, further comprising instruction interpretation means for interpreting an externally-input setting instruction to write at least one of the security release key and the security registration lock into the at least one memory region or the at least one non-volatile storage means, respectively.

Claim 4 (original): A semiconductor storage device according to claim 2, wherein the determination circuit compares the value which is generated based on the security release key against the value which is generated based on the security registration lock for each of the at least one memory cell array block, and results of comparison are collaterally written in the at least one register.

Claim 5 (original): A semiconductor storage device according to claim 1, further comprising a unidirectional conversion circuit or an encryption circuit, wherein results of converting the security release key and the security registration lock by means of the unidirectional conversion circuit or the encryption circuit are written to the at least one memory region and the at least one non-volatile storage means, respectively.

Claim 6 (original): A semiconductor storage device according to claim 1, which lacks means for reading the security release key and the security registration lock.

Claim 7 (original): A semiconductor storage device according to claim 1, wherein:

the at least one non-volatile storage means is a one-time programmable ROM which prohibits rewriting and erasure; and

rewriting and erasure are prohibited after the security registration lock is written.

Claim 8 (original): A semiconductor storage device according to claim 1, wherein:

the at least one non-volatile storage means is a one-time programmable ROM which prohibits rewriting and erasure; and

the semiconductor storage device has a non-volatile lock function for locking the semiconductor storage device to prohibit rewriting and erasure after writing of the security registration lock has been performed.

Claim 9 (original): A semiconductor storage device according to claim 1, further comprising a flag indicating that the security release key has been set,

wherein the flag is set automatically or manually after the security release key is written, thereby prohibiting additional writing to the corresponding one of the at least one memory cell array block.

Claim 10 (original): A semiconductor storage device according to claim 1, wherein a wait operation is performed while writing the security release key to the at least one memory region.